IN THE CLAIMS

The following is a complete listing of the claims, and replaces all earlier versions and listings.

1. (Currently Amended) Method of emulating a design under test associated with a test environment, the method comprising: ~~characterized in that it comprises two distinct generating phases comprising a first phase of~~

generating, in a first phase, ~~(80)~~ a first file ~~(FCH1)~~ for configuring the test environment, [[and]]

~~a second phase of~~ generating, in a second phase, ~~(81)~~ a second file ~~(FCH2)~~ for configuring at least a part of the design under test,

delivering ~~the delivery of~~ the first configuration file to a first reconfigurable hardware part ~~(BTR)~~ forming a reconfigurable test bench so as to configure the test bench, and

delivering ~~the delivery of~~ the second configuration file to a second reconfigurable hardware part ~~(EML)~~ so as to configure an emulator of the design under test,

wherein the first and second reconfigurable [[two]] hardware parts are ~~being~~ distinct and mutually connected.

2. (Currently Amended) Method according to claim 1, wherein ~~characterized in that~~ the first ~~generating~~ phase ~~(80)~~ comprises:

producing ~~the production (800) of~~ a logic circuit ~~(CRL)~~ comprising ~~consisting of~~ a network of logic gates, the logic circuit being [[and]] representative of the test environment and ~~as well as of the~~ compilation directives, and

compiling the ~~a compilation (801) of this~~ logic circuit in accordance with ~~having regard to~~ the compilation [[said]] directives, so as to obtain the first configuration file ~~(FCH1)~~.

3. (Currently Amended) Method according to claim 2, wherein ~~characterized in that~~ the test environment comprises a collection of drivers ~~(PLi)~~ and [[of]] monitors ~~(MNi)~~, and ~~in that~~ the production of the [[said]] logic circuit comprises the formation of hardware blocks in the form of networks of logic gates, these hardware blocks representing: interfaces of drivers/monitors of software stimulation, interfaces of drivers/monitors of real hardware stimulation, [[and]] drivers/monitors of emulated hardware stimulation, blocks for calculations of hardware triggers, ~~as well as~~ and a block for interfacing with the emulator of the design under test.

4. (Currently Amended) Method according to claim 3, wherein ~~characterized in that the phase of forming~~ the formation of the hardware blocks is effected

on the basis of statically defined networks of gates or of networks of gates which are generated dynamically by a software module.

5. (Currently Amended) Method according to any one of claims 1 to 4, wherein ~~characterized in that~~ the first ~~generating~~ phase ~~(80)~~ and the second ~~generating~~ phase ~~(81)~~ are performed in parallel.

6. (Currently Amended) Method according to any one of claims 1 to 4, wherein ~~characterized in that~~ the first ~~generating~~ phase ~~(80)~~ and the second ~~generating~~ phase ~~(81)~~ are performed sequentially.

7. (Currently Amended) Method according to claim 6, wherein ~~characterized in that~~ the first ~~generating~~ phase ~~(80)~~ is performed before or after the second ~~generating~~ phase ~~(81)~~.

8. (Currently Amended) Method according to claim 3, wherein ~~characterized in that~~

when the first ~~generating~~ phase is performed after the second ~~generating~~ phase, the production of the logic circuit ~~(CRL)~~ uses as input parameters a description of the assignment of the logic inputs/outputs of the design under test to the pins of the emulator, and

~~in that~~ when the second ~~generating~~ phase is performed after the first ~~generating~~ phase, the production of the logic circuit uses as input parameters a description of the interface of the design under test and supplies as output a description of the assignment of the logic inputs/outputs of the design under test to the pins of the emulator, ~~this~~ the output description ~~then~~ being used as a constraint parameter for the second ~~generating~~ phase.

9. (Currently Amended) Emulation system~~, intended to emulate~~ for emulating a design under test associated with a test environment, ~~characterized in that it comprises~~ the system comprising:

a host computer,

a reconfigurable hardware test bench ~~(BTR)~~ connected to the host computer and operable to emulate at least a part ~~capable of emulating a part at least~~ of the test environment, ~~this test bench being connected between a host computer and~~

a reconfigurable hardware emulator ~~(EML)~~, connected to and distinct from the test bench, and ~~capable of emulating~~ operable to emulate at least a part of the design under test,

first generating means ~~able~~ operable to generate a first file for configuring the test environment, and

second generating means ~~able~~ operable to generate a second file for configuring the design under test.

10. (Currently Amended) System according to claim 9, wherein ~~characterized in that~~ the reconfigurable test bench ~~(BTR)~~ comprises a [[so-called]] fixed part and at least one reconfigurable interface circuit ~~(CRFG) capable of~~ embodying the emulated part of the test environment.

11. (Currently Amended) System according to claim 10, wherein ~~characterized in that~~ the fixed part comprises at least one control circuit ~~(CCTL)~~ and one circuit ~~(CIBS)~~ for interfacing with the host computer, and ~~in that~~ the reconfigurable interface circuit comprises ~~is able to comprise at least~~ interfaces of drivers/monitors of software stimulation which are operable to establish ~~capable of establishing a~~ communication with at least one software process executed on the host computer, and drivers/monitors of emulated hardware stimulation.

12. (Currently Amended) System according to claim 11, wherein ~~characterized in that~~ the fixed part furthermore comprises ~~additional real~~ hardware drivers/monitors, and ~~in that~~ the reconfigurable circuit ~~(CRFG) is able furthermore to comprise~~ comprises interfaces with the ~~these additional real~~ hardware drivers/monitors.

13. (Currently Amended) System according to any one of claims 9 to 12, wherein ~~characterized in that~~ the fixed part ~~furthermore~~ comprises a circuit ~~(IFSC)~~ for interfacing with a target device ~~(SYC)~~.

14. (Currently Amended) System according to claim 9, wherein ~~characterized in that~~ the fixed part ~~furthermore~~ comprises ~~the~~ a control part of a hardware logic analyser ~~(AL)~~ whose state evolves as a function of the hardware triggers.

15. (Currently Amended) System according to claim 9, wherein ~~characterized in that~~ the reconfigurable test bench comprises a clock signals generator synchronized by a base system clock and delivering various secondary clock signals synchronizing the emulator of the design under test and certain at least of the hardware means of the test bench, the reconfigurable test bench further comprising ~~as well as~~ clock retrocontrol means operable to, ~~capable~~ in response to at least one wait signal transmitted by one of the hardware means of the test bench regulated by a first secondary clock signal, [[of]] temporarily disable ~~disabling~~ certain of the other secondary clock signals with different frequencies from that of the first secondary clock signal.

16. (Currently Amended) System according to claim 9, wherein ~~characterized in that~~ the test bench and the emulator are embodied on an electronic card

external to the host computer and connected to ~~the latter's~~ a mother card of the host computer.

17. (Currently Amended) System according to claim 9, wherein ~~to, characterized in that~~ the reconfigurable test bench is embodied on a first electronic card external to the host computer and connected to a ~~the latter's~~ mother card of the host computer, and ~~in that~~ the emulator of the design under test is embodied on one or more other cards external to the host computer and connected to the [[said]] first electronic ~~external~~ card.

18. (Currently Amended) System according to claim 17, wherein ~~characterized in that~~ the circuit for interfacing with the target device is integrated into the [[said]] first electronic ~~external~~ card.

19. (Currently Amended) System according to any one of claims 10 to 12, wherein ~~characterized in that~~ the test bench and the emulator are embodied on an internal electronic card (CINT) incorporated into the host computer.

20. (Currently Amended) System according to claim 13, wherein ~~characterized in that~~ the circuit for interfacing with the target device is embodied on an

external electronic card ~~(CXT)~~ outside the host computer, and configured ~~able~~ to be connected to the [[said]] internal electronic card ~~(CINT)~~.

21. (Currently Amended) An apparatus in the form of an electronic ~~Electronic~~ card~~, intended~~ configured to be connected to the mother card of a host computer, ~~characterized in that it comprises~~ the electronic card comprising:

a reconfigurable hardware test bench ~~(BTR) capable of emulating a part at least~~ operable to emulate at least a part of a test environment associated with a design under test, and

a reconfigurable hardware emulator ~~(EML)~~, distinct from the test bench, connected to the reconfigurable test bench and ~~capable of emulating~~ operable to emulate at least a part of the design under test.

22. (Currently Amended) The apparatus ~~Card~~ according to claim 21, wherein ~~characterized in that~~ the reconfigurable test bench ~~(BTR)~~ comprises a [[so-called]] fixed part and at least one reconfigurable circuit ~~capable of embodying~~ operable to embody the emulated part of the test environment.

23. (Currently Amended) The apparatus ~~Card~~ according to claim 22, wherein ~~characterized in that~~ the fixed part comprises at least one control circuit ~~(CCTL)~~ and one circuit for interfacing with the host computer, and ~~in that~~ the reconfigurable circuit

~~is able to comprise at least~~ comprises interfaces of drivers/monitors of software stimulation which are ~~capable of establishing a~~ operable to establish communication with at least one software process executed on the host computer, and drivers/monitors of emulated hardware stimulation.

24. (Currently Amended) The apparatus ~~Card~~ according to claim 23, wherein ~~characterized in that~~ the fixed part furthermore comprises ~~additional real~~ hardware drivers/monitors, and ~~in that~~ the reconfigurable circuit ~~is able to comprise further~~ comprises interfaces with the ~~these additional real~~ hardware drivers/monitors.

25. (Currently Amended) The apparatus ~~Card~~ according to any one of claims 21 to 24, wherein ~~characterized in that~~ the reconfigurable test bench comprises a clock signals generator synchronized by a base system clock and delivering various secondary clock signals of different frequencies, the reconfigurable test bench further comprising ~~as well as~~ clock retrocontrol means operable to, ~~capable~~ in response to a wait signal transmitted by one of the hardware means of the test bench regulated by a first secondary clock signal, [[of]] temporarily disable ~~disabling~~ the secondary clock signals with different frequencies from that of the first secondary clock signal.